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A survey on router in bufferless NoC.

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ABSTRACT

Network on-Chip (NoC) is a novel technology which is used to make the interconnections between the components available in the System on Chip (SoC) design. In network on chip, routing is the technique to select the better path among the available path. It has different types of algorithm to improve the performance such as throughput, area minimization and power minimization. In general, NoC with buffer consumes more area and that is considered to be more delay. Hence, it was proposed a bufferless NoC. In this paper, the NoC without buffer with mesh topology is taken and whole performance of NoC router network is discussed for the overall idea of NoC Routing technique for various VLSI design.

Keywords: Routing technique, Network on chip, System on chip, Bufferless Routing, VLSI design

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INTRODUCTION

In data or packet transaction networks, the routing mechanism is the major impact on the performance of the whole network. Even though many techniques are present in the network the routing have the major part in the performance side. Intermediate nodes and the other nodes make the communication by buses, routers, bridges are used to communicate with in the nodes. The Area, latency, power consumption and throughput plays a vital role in the bufferless routing network algorithm. Now in the router technique the bufferless NoC is improving for development of the router in performance. Our demand for unbuffered communication converts the chatting problem to a pure scheduling problem. This demand is shared with the regimen of hot potato (or, deflection) routing. It appears also in the study of scattering and gathering general messages in general networks, in this router plays a vital role.

The router network have topologies like mesh topology, Torus, Hypercubes topology. In this mesh topology is taken into consideration. Each processor is connected with the one router which acts as a bus and passes the data through the router. Each router have five ports if one or more port is free the processor eject the data. Normally, the path of the router is mentioned in the typical algorithm. Then it is necessary to check the traffic or all port availability. When the load is normal, then the router function takes place without problem. But when the port availability is less and packets are passing continuously then the deflection forms and the unwanted use of resource takes place. In this condition, it is necessary to move to different optimizing algorithm. As the VLSI problem comes, all problems cannot be solved in a single algorithm. One or two problems is solved with the penalty of other. Even though the problem should overcome with maximum optimization. To achieve the maximum optimization many algorithm is need to be reviewed. As move to many algorithm, BLESS algorithm is common and basic building block algorithm for the bufferless router. The enhancement for the performance of the router is done by improving the BLESS algorithm or the results are compared by this algorithm.

BLESS Algorithm

BLESS Algorithm is simply said as bufferless algorithm and it eliminates the storage of the packet since storage element (buffer) is eliminated. so the router is no need to wait for any response. Since in mesh topology there will be five ports maximum for the one router. The packets which is transmitted will assign to any one among the five port. If any other topology is considered then the number of ports will be differed. According to the topology the packet is assigned in the ports. Productive links and non-productive links are present in the router. If the packet is assigned to the link near to the destination is said to be productive link and the link far away from the destination is said to be non productive. This algorithm is initiative for the bufferless routing algorithm. Then many algorithm is developed to increase the performance of this algorithm.

Throughput Enhancement

Throughput means the number of packets per unit time. It is improved by different technique used in the router. By improving the throughput, it is considered to be performance improvement. In any algorithm, throughput plays an important role. It is mandatory to improve. The various bufferless algorithm are discussed to overcome this problem.

Chipper

In the first bufferless algorithm BLESS the main disadvantage is deflection. Which means if the packets passed through the nodes if all the ports are busy with another packets. Then the packet will be continuously deflected till any one of the port is free. To avoid such a unwanted deflection the chipper method is introduced. In this for the particular time called 'golden epoch' each packet is considered to be the 'golden packet'. In particular clock period that packet should be delivered. For each and every node this time is allocated and they are delivered at the particular time.

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An extended routing table method

In this method of routing, the bufferless routing is considered by adding some less modification to achieve throughput. Already existing protocols are random routing methods and RIP[2]. In this, it may consider to have extended tables, which have number ports with priority. From the table the priority of the packets are assigned to the ports and if the previous packet is assigned to the priority address and the other packets are deflected outwards away to the destination. But the assignment of the packet is already done. Hence the router increases the throughput. Packet loss probability is given in the fig:2. The architecture of bufferless routing based on packet deflection can be a promising candidate for the next generation high-throughput networks.

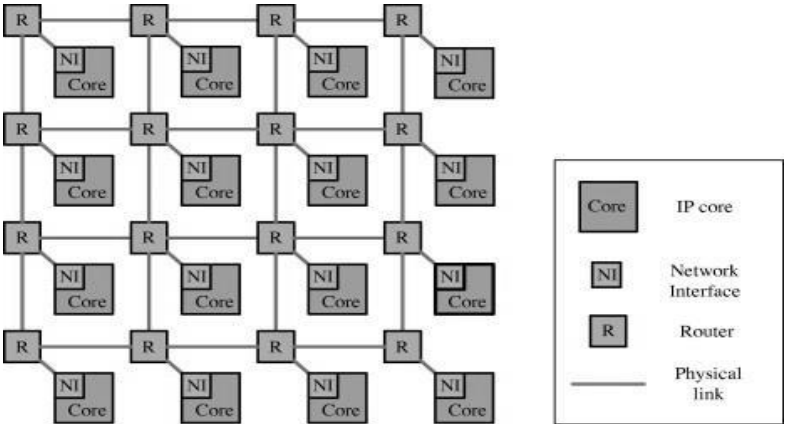

Figure 1: Network on Chip

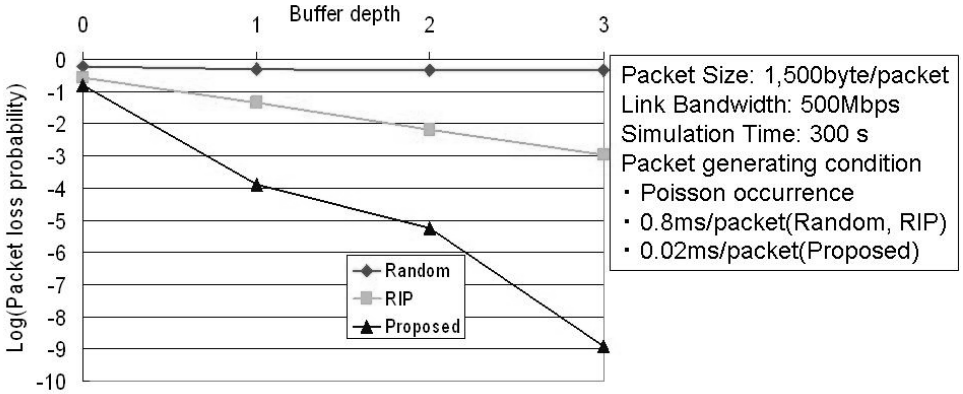

Figure 2: Packet loss probability

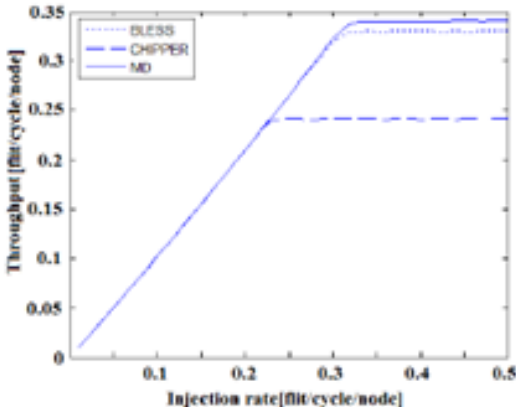

Figure 3: Injection rate Vs Throughput

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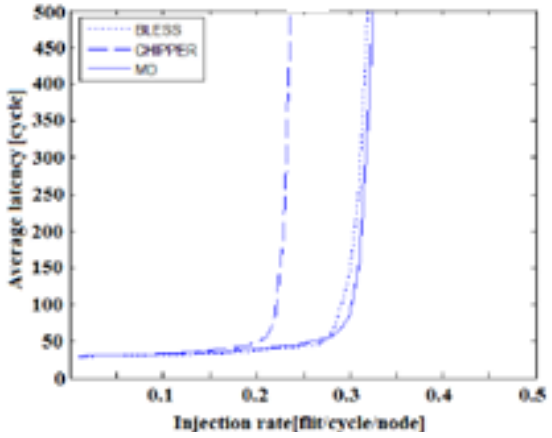

Figure 4: Injection rate Vs Average Latency

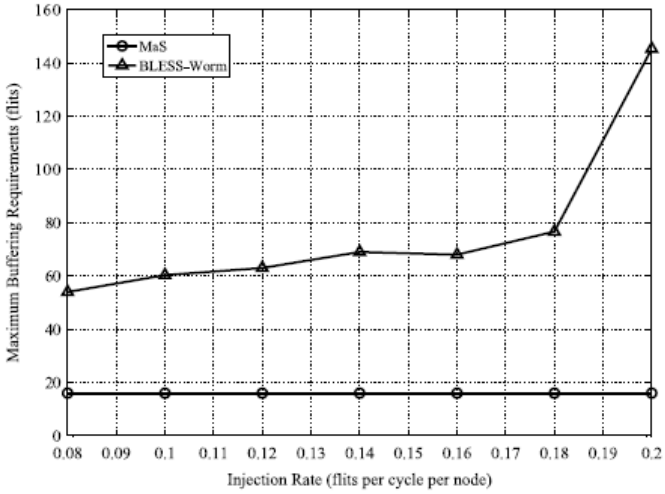

Figure 5: Buffering area minimization in MaS

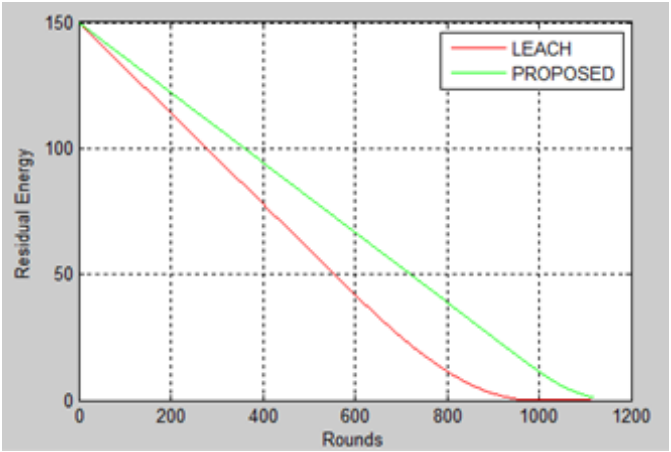

Figure 6: Evaluation of energy consumption

A co-ordinate routing method

To evaluate this method of routing, normal grid type is enough to experiment simply. No need of extended tables. In each grid type, router is placed and the distance is calculated from source to destination[2]. The packet loss probability can be decreased by increasing the number of outgoing links from each routing node. Various network topologies consisting of higher than 4 degree nodes will be examined through this method. The calculated distance is noted and the packet is assigned to the free port with shortest path. In this instead of IP address, co-ordinates are considered.

Minimum Deflection

Minimum deflection is the way to reduce the number of deflection in the router. The Normal deflection does not compare priority of packets. It blankly passes the unoccupied nodes to the another port. By doing this the number of the deflection increases. So that the performance reduces. To overcome this minimum deflection is used as the solution. During deflection it does not blankly pass the packets it selects the nearer node and then it assign the port.

Latency Improvement

Average latency is the time delay between inserting the packet into network and ejected from network. In other words, it can be taken as, processing time between inject and eject of the networks. Many algorithm and techniques are take for the latency improvement. Latency also takes the important place to improve the performance of the bufferless router.

SCARAB Architecture router Pipeline

The Single Cycle Adaptive Routing and Bufferless Network is shortly called as SCARAB in the routing. This router works by the simple single pipeline to improve the performance in the part of latency. The header in the packet travels towards the small network single cycle along with the data. By minimizing the operator of the network with a single-cycle latency, trailing its on the data network the latency is reduced by single cycle. The NACK stands for the negative acknowledgement. In order to reduce the negative acknowledgement the unavailable output ports are masked[11]. Then the number of possible requests are counter and the number of outputs and the available ports are more, then it is considered. Computes the maximum priority request port. According to the priority the winning node passes the packet. The NACK signal of respected packet is assigned to the node before to the previous node. The signal coming from the NACK is traveled again from the source to destination for the retransmission of the packets to overcome the deflection packets. The NACK signal is taken as the already configured circuit in router network. It is a only one delay from input to output.

Span Design

Span design elects all the co-ordinates for the all nodes in the networks. It is always in active conditions and they always performs the multi-hop packet routing[10]. At first, it takes the required co-ordinates. It rotates the co-ordinates to take enough co-ordinates in order to share the task provided by the whole connectivity. By this sharing of task the processing time is decreased and the latency is improved. Then it drastically reduce the nodes which are elected. Then the local information are decentralized. To calculate the empowerment of Span algorithm, the simulation with Span and forwarding mechanism, on many movable and immovable topologies are taken as the results. Simulation results of the designs show that Span is not only suitable for the performance of router but also increase the performance in power sector and saves the router network lifetime and optimize the latency of the single packet.

Area Empowerment

To reduce the area and cost efficiently by removing input buffers of the router is However, it is evident that this performance gets jammed at high loads because of the increase in the network contentions and deflection of packets in huge amount. Now a days the area should be reduced in all the components. Since the user required compact product to use and that should be portable. To reduce the amount of deflection

and to improve the performance various algorithm is used discussed. In area optimization the best algorithm is MaS algorithm**.**

Mas bufferless algorithm in routing

The Mas routing algorithm is introduced to reject the buffers in all routers. The main advantage is to limit the livelock problem in the routers from the deflection. Livelock problem is more in the routers and it is necessary to reduce or reject the livelock problem in all routing techniques. In MaS the priority less port packets are stopped or stored in the register array near the port. For example if the packet P1 is in east side and also another packet need to choose the same side east. Then by comparing the priority, if the packet P1 is less priority then the P1 packet is registered in the nearby array. By comparing the BLESS-Worm algorithm with MaS algorithm the area of the buffer is reduced in the receiver side and power also reduced in small amount[1]. From this to minimize the area of the router MaS is suggested. In area empowerment only one type is suggested. Hence it gives 80% improvement in the area side. It is better to discuss and take this type for the further process.

Power Efficiency

In routing, particularly in NOC routing the power is most used resource. While the packet travelling from one node to another sometimes it may jammed or roamed due to the occupied port. Since the packet is movable till eject the power used more. In order to reduce the power consumed by the packet, the unnecessary packet movement or deflection of the packet should be reduced or the packet should be ejected. Hence some algorithm are suggested for the betterment of performance. Now a days the wireless products are improved in large number. All products are manufactured for compact and portable facility. In order to carry the product it is necessary to save the power and to reduce the power consumption in more application. Since many algorithm are developed for the performance. Many algorithms are proposed to reduce the power consumption by the router to improve the performance of the router. Static power may become the dominant power problem in Networks-on-Chip (NoCs). Since the technology is narrow down to the nano scale. Even more the static power becomes the major factor to be reduced. Powergating is an efficient technique to reduce the static power of under-utilized resources in different types of circuits. Even more techniques are giving better results than the power gating. In addition some different techniques are discussed.

Clumsy Flow Control (CFC)

The CFC minimize the congestions of the in the network and also improves the performance of the bufferless router. It is also extended to the Dynamic CFC for the betterment of the router algorithm during execution[3]. This is extended to randomized-deterministic allocation(RDA) in addition to reduce the critical path. In general, all the packets are partitioned into one or more flits while it is set for transmission and width of the buffer entry represents the flit width. The above concept of CFC is introduced into a bufferless NOC. This is called as an inexact destination and credit based flow control which is used to avoid the blocking between the networks and also to reduce the deflection.

FLIT- BLESS Algorithm

The FLIT - BLESS routing strategy is based on ranking. In each rotation, using the component of flit ranking, the incoming flits are ranked. The free output ports are ranked according with the priority with desirability. The router normally assign the flit accordingly with the priority which is the higher priority first and the least priority next in certain order of flit assignments. This increases the energy efficiency and eliminate the complex buffer management[4]. In this the five different flits are taken and the packets are assigned according to the flit selected. The first flit is Oldest First (OF), the second one is Closest First (CF), third one is Most Deflections First(MDF), fourth one is Round Robin(RR) and the last one is Mixed Policy(MP). By considering the above mentioned flits the routing is done and the decision is taken to save energy.

BLESS Wormhole Routing

In WORM-BLESS, port prioritization of required port is difficult to overcome livelocks. Generally to follow the key which is not vary that the OF(oldest flit) in the router moreover made the process into their destination, the worms are applied in some cases for truncation. The rule of router port-prioritization gives the different between the head-flits and the non-head flits. In the head-flit, a different output port should be given[4]. By Employing the mentioned mechanism reduction of some negligible energy will be taken at largest performance reduction which is compared to buffered routing techniques, The volume of the injected traffic port is not too much large, which is in high real applications cases[4]. In flit based the latency is high since it has five flits, it have to select then process. But in the wormhole routing, the packet have the header information and it have the data to select any one of the flit for the particular packets.

CONCLUSION

In this survey the different types of bufferless algorithms and techniques are discussed and the improvement of the performance also represented for the further process. The performance are improved by taking any of the algorithm or the combination may also try to get the better results for future work. As the real problems comes the solutions will give the proper better results. It gives the overall working mechanism of the bufferless routing in the NOC for efficient outcome to overcoming VLSI problems. VLSI gives different kinds of problem and this survey gives various methods as the solution to overcome those problems. This survey will avail the incipient readers to understand the concept of various routing techniques for better performance.

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